IN THE CLAIMS:

1-2. (Canceled)

3. (Currently Amended) ~~The layout check system of claim 2, wherein~~ A layout check system that checks layout data that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising:

a storage unit operable to store the layout data, the layout data including information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second value corresponding to impedance between the power pin and the bypass capacitor;

a calculation unit operable to calculate, with use of the layout data, a shortest wiring distance between the power pin and the power source as a first value, and a shortest wiring distance between the power pin and the bypass capacitor as a second value;

a judgment unit operable to judge, by comparing the first value with the second value, that the layout does not allow the bypass capacitor to function effectively if the first value is less than the second value; and

an output unit operable to output error information when a result of the judgment is negative,

wherein when a power via exists on wiring that connects the power pin and the bypass capacitor, the calculation unit calculates, with use of the layout data, a shortest wiring distance between the power pin and the power via as the first value, and the shortest wiring distance between the power pin and the bypass capacitor as the second value.

4. (Canceled)

5. (Currently Amended) ~~The layout check system of claim 1 wherein~~

~~the layout data includes type information that indicates whether wiring is a line or a plane, and, for wiring that is in a plane, further includes area information indicating a surface area of the plane,~~

~~the storage unit stores a prescribed value,~~

~~the layout check system further includes:~~

~~an analysis unit operable to analyze, with use of the type information, whether wiring connects the power pin and the bypass capacitor is a line or a plane; and~~

a layout check system that checks layout data that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising:

a storage unit operable to store the layout data, the layout data including (a) information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second value corresponding to impedance between the power pin and the bypass capacitor, (b) type information that indicates whether wiring is a line or a plane, and (c) area information indicating a surface area of the plane, and further operable to store a prescribed value;

a calculation unit operable to calculate the first value and the second value, with use of the stored layout data;

a judgment unit operable to judge, by comparing the first value with the second value, whether the layout allows the bypass capacitor to function effectively;

an output unit operable to output error information when a result of the judgment is negative;

an analysis unit operable to analyze, with use of the type information, whether wiring that connects the power pin and the bypass capacitor is a line or a plane; and

a power plane judgment unit operable to judge, when a result of the analysis indicates that the wiring that connects the power pin and the bypass capacitor is a plane, whether the surface area of the plane is less than the prescribed value, by referring to the area information, and when the surface area is less than the prescribed value, judge that the plane is a specific power plane, [[and]] wherein

when the power plane judgment unit judges the wiring to be the specific power plane, the analysis unit further analyzes, with use of the layout data, whether the specific power plane and the power source are connected without a bypass capacitor therebetween, and when a result of the analysis indicates that the specific power plane and the power source are connected without a bypass capacitor therebetween, judge that the layout is not a layout that allows a bypass capacitor to function effectively.

6. (Currently Amended) A layout check method for checking layout data that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising:

an obtaining step of obtaining layout data, the layout data including (a) information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second value corresponding to impedance between the power pin and the bypass capacitor, (b) type information that indicates whether wiring is a line or a plane, and (c) area information indicating a surface area of the plane, and further operable to store a prescribed value;

a calculation step of calculating the first value and the second value, with use of the layout data;

a judgment step of judging, by comparing the first value with the second value, whether the layout allows the bypass capacitor to function effectively; [[and]]

an output step of outputting error information when a result of the judgment is negative [[.]];

an analysis step of analyzing, with use of the type information, whether wiring that connects the power pin and the bypass capacitor is a line or a plane; and

a power plane judgment step of judging, when a result of the analysis indicates that the wiring that connects the power pin and the bypass capacitor is a plane, whether the surface area of the plane is less than the prescribed value, by referring to the area information, and when the surface area is less than the prescribed value, judge that the plane is a specific power plane, wherein

when the power plane judgment step judges the wiring to be the specific power plane, the analysis step further analyzes, with use of the layout data, whether the specific power plane and the power source are connected without a bypass capacitor therebetween, and when a result of the analysis indicates that the specific power plane and the power source are connected without a bypass capacitor therebetween, judges that the layout is not a layout that allows a bypass capacitor to function effectively.

7. (Currently Amended) A program that has a computer execute layout check processing for checking layout data that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising:

an obtaining step of obtaining layout data, the layout data including (a) information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second value corresponding to impedance between the power pin and the bypass capacitor, (b) type information that indicates whether wiring is a line or a plane, and (c) area information indicating a surface area of the plane, and further operable to store a prescribed value;

a calculation step of calculating the first value and the second value, with use of the layout data;

a judgment step of judging, by comparing the first value with the second value, whether the layout allows the bypass capacitor to function effectively; [[and]]

an output step of outputting error information when a result of the judgment is negative[.];

an analysis step of analyzing, with use of the type information, whether wiring that connects the power pin and the bypass capacitor is a line or a plane; and

a power plane judgment step of judging, when a result of the analysis indicates that the wiring that connects the power pin and the bypass capacitor is a plane, whether the surface area of the plane is less than the prescribed value, by referring to the area information, and when the surface area is less than the prescribed value, judge that the plane is a specific power plane, wherein

when the power plane judgment step judges the wiring to be the specific power plane, the analysis step further analyzes, with use of the layout data, whether the specific power plane and the power source are connected without a bypass capacitor therebetween, and when a result of the analysis indicates that the specific power plane and the power source are connected

without a bypass capacitor therebetween, judges that the layout is not a layout that allows a bypass capacitor to function effectively.

8. (New) A method for checking the effectiveness of a bypass capacitor in a circuit board layout, comprising the steps of:

reading information about a power source, a bypass capacitor, an integrated circuit (IC) power pin and wiring connections between them, including whether a line or a plane comprises the wiring and surface area of the plane;

determining from the information if the bypass capacitor and the IC power pin have a common power node;

calculating, when a common power node exists, an impedance from the common power node to the bypass capacitor from the information;

calculating, when a common power node exists, an impedance from the common power node to the IC power pin from the information;

comparing the impedance of the common power node to the bypass capacitor with the impedance from the power node to the IC power pin; and

outputting an output result of the comparison;

whereby the output determines whether the bypass capacitor in the circuit board layout will be effective at suppressing parasitic noise and power fluctuations at the IC power pin.

9. (New) The method of claim 8 wherein the common power node is at one end of a power via.

10. (New) The method of claim 8 wherein the output is an error message if the common power node to IC power pin impedance is larger than the common power node to the bypass capacitor impedance.

11. (New) The method of claim 8 wherein the circuit board layout impedances are calculated by using line lengths of the wiring connections.

12. (New) The method of claim 11 wherein the result is an error message if the common power node to IC power pin line length is longer than the common power node to the bypass capacitor line length;

13. (New) The method of claim 8 further comprising the steps of:

reading information about all bypass capacitors in the circuit board layout;

determining if each bypass capacitor and the IC power pin have a common power node;

calculating the impedances for each common power node to each respective bypass capacitor;

calculating the impedances from each common power node to the IC power pin;

comparing the impedances from each common power node to the IC power pin with the respective impedances for each common power node to each respective bypass capacitor; and

outputting the result of the comparisons.